Amendments to Claims:

This listing of claims will replace prior versions of claims in the application:

1. (canceled)

2. (withdrawn) The package of claim 1, wherein the plurality of electrical connections between the die bond pads and the package bond pads are made by wirebonds.

3. (withdrawn) The package of claim 1, wherein the plurality of electrical connections between the die bond pads and the package bond pads are made by TAB

4-18 (canceled)

19. (new) A semiconductor package comprising

an integrated circuit die with a plurality die bond pads,

a printed wiring board,

with a plurality of package bond pads,

with a plurality of package pads,

with electrical circuitry of a plurality of voltages, connecting the selective package bond pads to respective selected package pads, with a plurality of conductive traces, or conductive planes,

a recess in the printed wiring board,

to attach the die,

to contain the plurality of die bond pads and plurality of package bond pads,

where the electrical circuitry is available across the total area of the recess, including under the die,

where there are a plurality of metallic vias in the printed wiring board and under the die, to conduct heat away from the die.

with the recess formed by bending or deforming the printed wiring board,

a plurality of electrical connections between the plurality of die bond pads and the plurality of package bond pads

20. (new) The package of claim 19, wherein the plurality of electrical connections between the die bond pads and the package bond pads are made by solder balls..

21. (new) The package of claim 19, wherein the printed wiring board has a metal core, one or more build-up layers and a solder mask passivation layer, where each buildup layer comprises an organic dielectric layer with vias and a patterned metal layer.

22. (new) The package of claim 21, wherein the circuitry of the printed wiring board is on one side, and the printed wiring board does not contain through vias or plated through holes (PTHs).

23. (new) The package of claim 21, wherein the metal core is made from a material which has a TCE to match an electronic board on which the semiconductor package is mounted.

24. (new) The package of claim 23, wherein the material is copper or aluminum.

25. (new) The package of claim 21, wherein the metal core is made from a material with a TCE to match the integrated circuit die.

26. (new) The package of claim 25, wherein the material is CuW, Mo, CuMo, copper clad Mo, Invar, and copper clad Invar.

27. (new) The package of claim 21, wherein the metal core is made from a material with a TCE half way between the integrated circuit die and the electronic board on which the semiconductor package is mounted.

28. (new) The package of claim 27, wherein the material is stainless steel.

29. (new) The package of claim 19, wherein there are a plurality of package solder balls attached to respective selected package pads.

30. (new) A method to fabricate the package of claim 19, wherein the printed wiring board has a metal core, one or more build-up layers and a solder mask passivation layer, where each buildup layer comprises an organic dielectric layer with vias and a patterned metal layer.

31. (new) A method to fabricate the package of claim 19, wherein the circuitry of the printed wiring board is on one side, and the printed wiring board does not contain through vias or plated through holes (PTHs).